Amendment to the specification

Please amend the paragraph on page 1 entitled "related applications:" such that the results are as follows:

Related Applications:

1) The current non-provisional application claims priority from provisional application 60/221,821 entitled "Traffic Stream Processor" filed on July 31, 2000.

2) The current application is a continuation of the non-provisional application 09/639,915 entitled "Integrated Circuit that Processes Communication Packets with Scheduler Circuitry that Executes Scheduling Algorithms based on Cached Scheduling Parameters", now pending, filed on August 16, 2000 which claims priority of the provisional application number 60/149,376 filed on 8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications".

3) The current application is a continuation of the non-provisional application 09/640,258 entitled "Integrated Circuit that Processes Communication Packets with Co-Processor Circuitry to Determine a Prioritized Processing Order for a Core Processor" filed on August 16, 2000, now patent number 6,754,233, which claims priority of the provisional application number 60/149,376 filed on 8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications."

4) The current application is a continuation of the non-provisional application 09/640,231 entitled "Integrated Circuit that Processes Communication Packets with Co-Processor Circuitry to Correlate a Packet Stream with Context Information" filed on August 16, 2000, now patent number 6,804,239, which claims priority of the provisional application number 60/149,376 filed on 8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications."

The content of the above applications is hereby incorporated herein by reference.

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Please amend the paragraph starting on line 17 of page 3 such that the results are:

Co-pending applications 09/639,966, now patent number 6,760,377, 09/640,231, now patent number 6,804,239, and 09/640,258, now patent number 6,754,233 the content of which is incorporated herein by reference, describe an integrated circuit for processing communication packets. As described in the above applications, the integrated circuit includes a core processor. The processor handles a series of tasks, termed "events". These events consist of tasks such as CPU processing steps as well as the scheduling of subsequent events. These subsequently scheduled events may consist of CAM lookups, DMA data transfers, or other generic events based on conditions in the current event. All events have an associated service address, "context information" and "data". Information about the event such as the resource that requested the event, how much data is associated with the event, and other key information from the event requestor is stored in "special state" information associated with the event. When an external resource initiates an event, the external resource supplies the core processor with a memory pointer to "context" information and it also supplies the data to be associated with the event.

Please amend the paragraph starting on line 29 of page 6, continuing on page 7, such that the results are:

One embodiment of the present invention described herein is applied as an improvement to the type of integrated circuit described in co-pending patent applications 60/211,863 filed on June 14, 2000, 09/640,260, now pending, filed on August 16, 2000, 09/639,915 filed on August 16, 2000, 09/639,966, now patent number 6,760,377, filed on August 16, 2000, 09/640,258, now patent number 6,754,223, filed on August 16, 2000 and 09/640,231, now patent number 6,804,239, filed on August 17, 2000, the content of which is hereby incorporated herein by reference in order to shorten and simplify the description of the present application.

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